



Department of Electrical  
and Computer Engineering

## ELE 305: Introduction to Electrical Engineering Final Exam – Spring 2017

Duration: **2 hours 30 minutes**

Date: 06/05/2016

Start Time: 8:00 am

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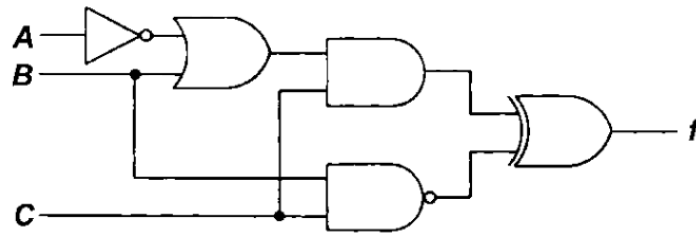
### INSTRUCTIONS:

- Answer each of the following questions in the space provided.
- You can use both sides of the sheets for answers.
- Solutions written outside this booklet will not be graded.
- This is a closed-book exam
- Programmable calculators and smart devices are not allowed.
- The number of points for each question is specified next to it.
- The total number of points is 100.

1	2	3	4	5	6	7	Total
/22	/14	/8	/14	/12	/14	/16	/100

**Question 1 (22 pts)**

- I. Convert the number 10010110 into a decimal number, if it was [6pts]
  - a. an unsigned binary number
  - b. a binary coded decimal
  - c. an 8-bit 2's complement
  
- II. Convert the binary number 1011.0011 to [6pts]
  - a. A decimal number
  - b. An octal number
  - c. A hexadecimal number
  
- III. Write the standard expression for **f** in terms of **A**, **B** and **C** for the following logic circuit [4pts]:



**Figure 1**

- IV. Determine the minimum SOP expression for a function F with the following karnaugh map [6pts]:

CD \ AB	00	01	11	10
00	1	1	1	
01	1	1	1	
11			1	
10				



**Question 2 (14 pts)**

A game of rock paper scissors is to be implemented as a logic circuit. This hand game is played between 2 players such that each player has the option to choose rock, paper or scissors whereby rock beats scissors, scissors beats paper and paper beats rock.

The logic circuit would have two words as inputs, each word represents the choice of one player (00 if rock, 01 if paper and 10 if scissors). The output of the circuit is a single bit that is **true** if player 1 beats player 2 or both players are tied and **false** if player 2 is victorious or one of the inputs is an invalid term.

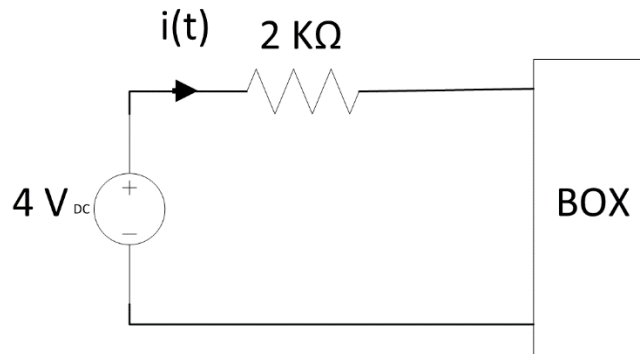
- a) Build the truth table for the game including all input bits and the output. [6pts]
- b) Using a karnaugh map, write a minimum SOP expression for the output in terms of the input bits. [8pts]



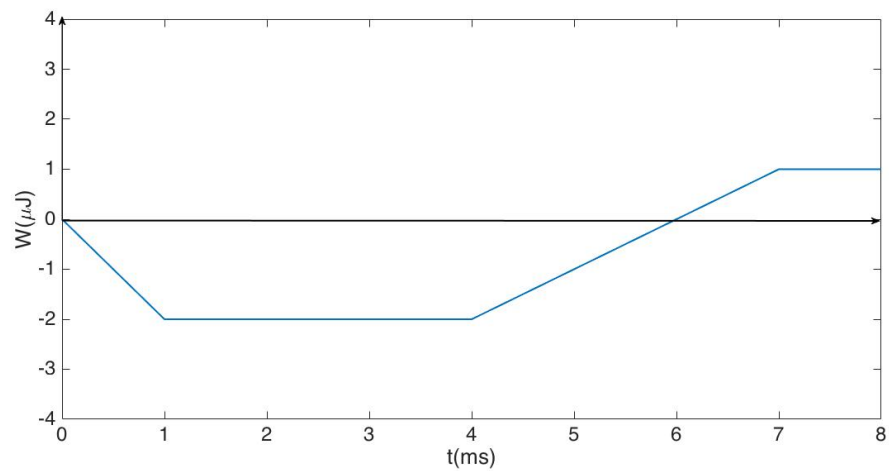
**Question 3 (8 pts)**

The energy consumed by the source in Figure 2.a is given by the waveform in Figure 2.b.

- Calculate and sketch the current  $i(t)$  [4pts]
- Calculate the average power consumed by the box over the period  $t=0$  to 8ms [4pts]



**Figure 2.a**



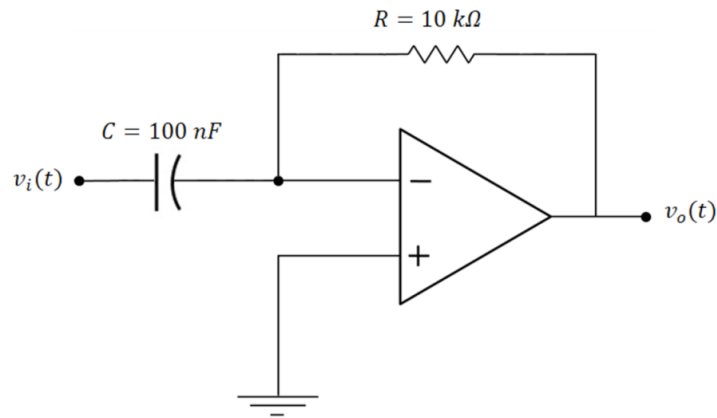
**Figure 2.b**



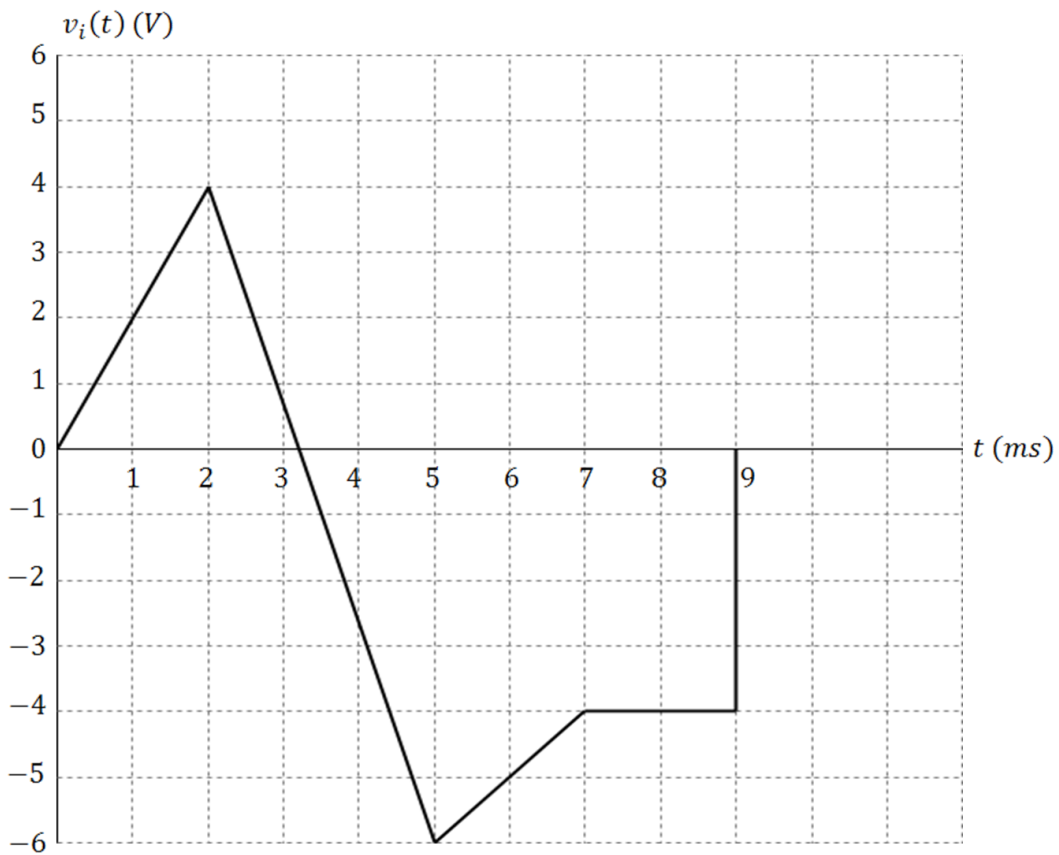
**Question 4 (14 pts)**

The input to the network shown in Figure 3.a is given by the waveform in Figure 3.b. The operational amplifier is considered ideal.

- a) Find an expression of  $v_o(t)$  in terms of  $v_i(t)$ . [10pts]
- b) Draw, on the same graph of Figure 3.b., the output waveform  $v_o(t)$ . [4pts]



**Figure 3.a**



**Figure 3.b**

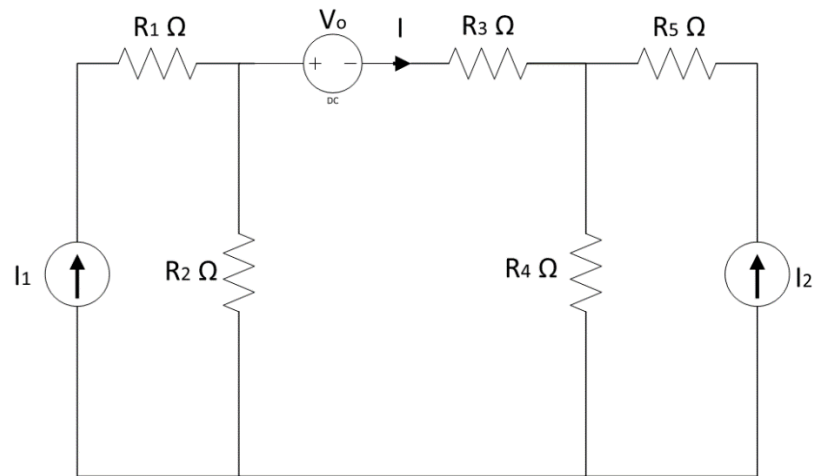




**Question 5 (12 pts)**

Consider the circuit in Figure 3.

- Find an expression for  $I$  using superposition. [10pts]
- Suppose  $R_2 I_1 = R_4 I_2$ . Is the voltage source  $V_o$  absorbing or supplying power? [2pts]



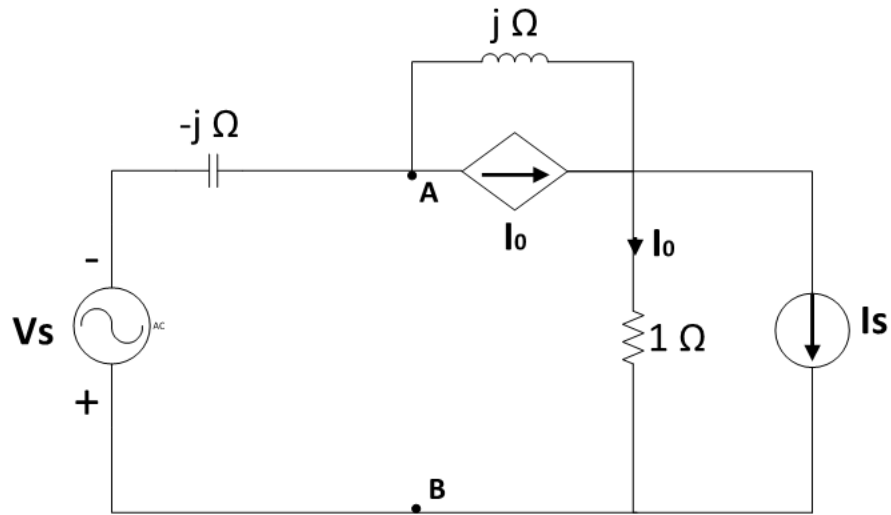
**Figure 3**



**Question 6 (14 pts)**

Find the thevenin equivalent of the circuit in Figure 4 as seen between points A and B.

$V_s = 1 \angle 180^\circ$  and  $I_s = 2 \angle -90^\circ$



**Figure 4**



**Question 7 (16 pts)**

A 480 V *rms*, 60 Hz voltage source delivers power to three loads in parallel:

- Load A: Purely resistive load of 4 kW.
  - Load B: Inductive load, 28 kVA at 0.707 power factor.
  - Load C: Capacitive load, 2 kW and 2 kVar.
- a. Find the total power, the total reactive power, the power factor for the source, and the *rms* source current. [10pts]
- b. A fourth load that is purely capacitive is connected in parallel with the above loads making the new overall power factor 0.9 lagging.
- i. Determine the reactive power absorbed by this capacitor and the value of the capacitance in Farads. [4pts]
  - ii. Calculate the new *rms* source current, what do you notice? [2pts]

